010327-007410US
George B. F. Yee, Reg. No. 37,478
Telephone: 650-326-2400
Inventor: John Marino
Title: Hardware Implementation of an N-Way Dynamic Linked List
Sheets of drawings 1 of 10

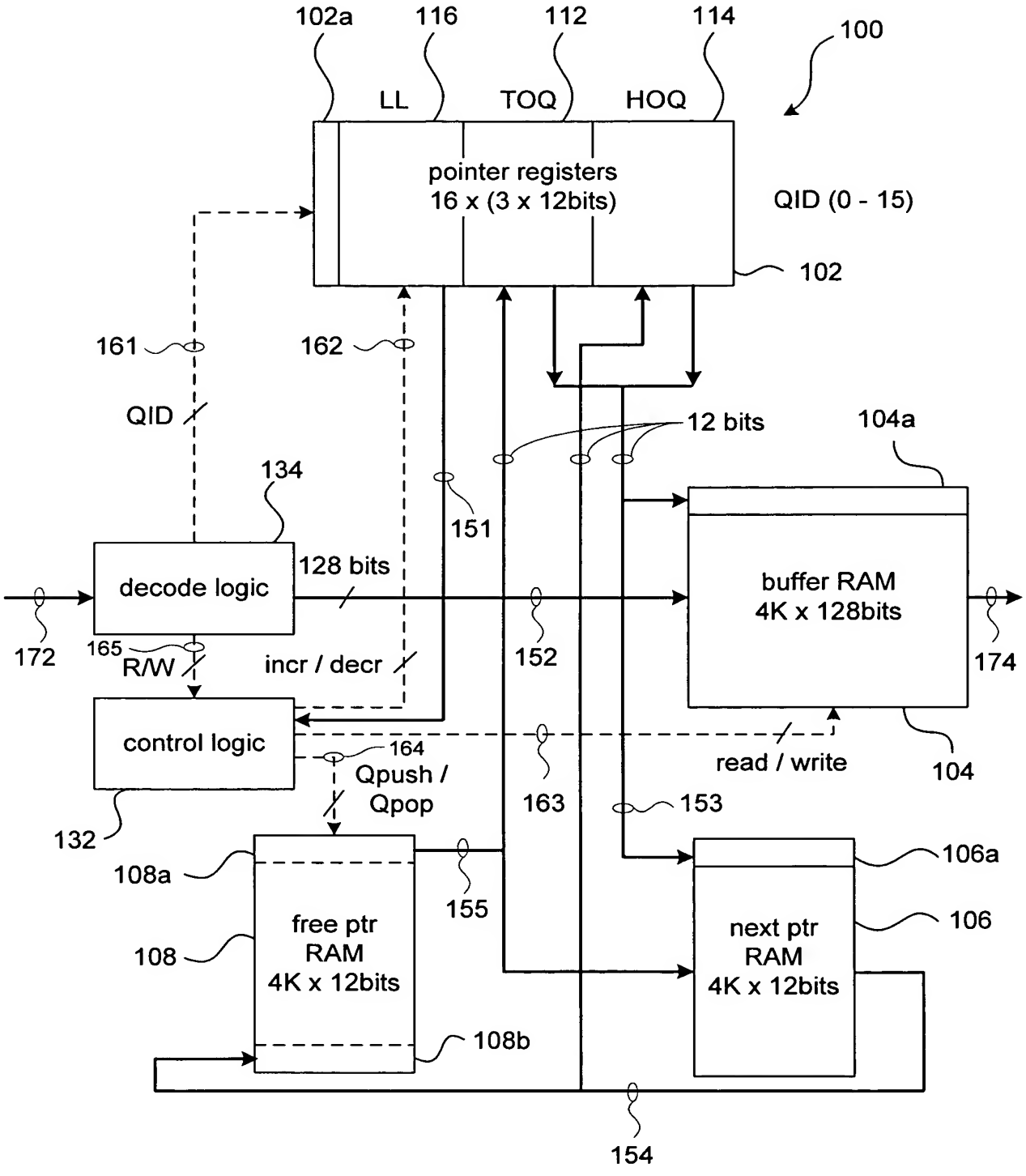

Fig. 1

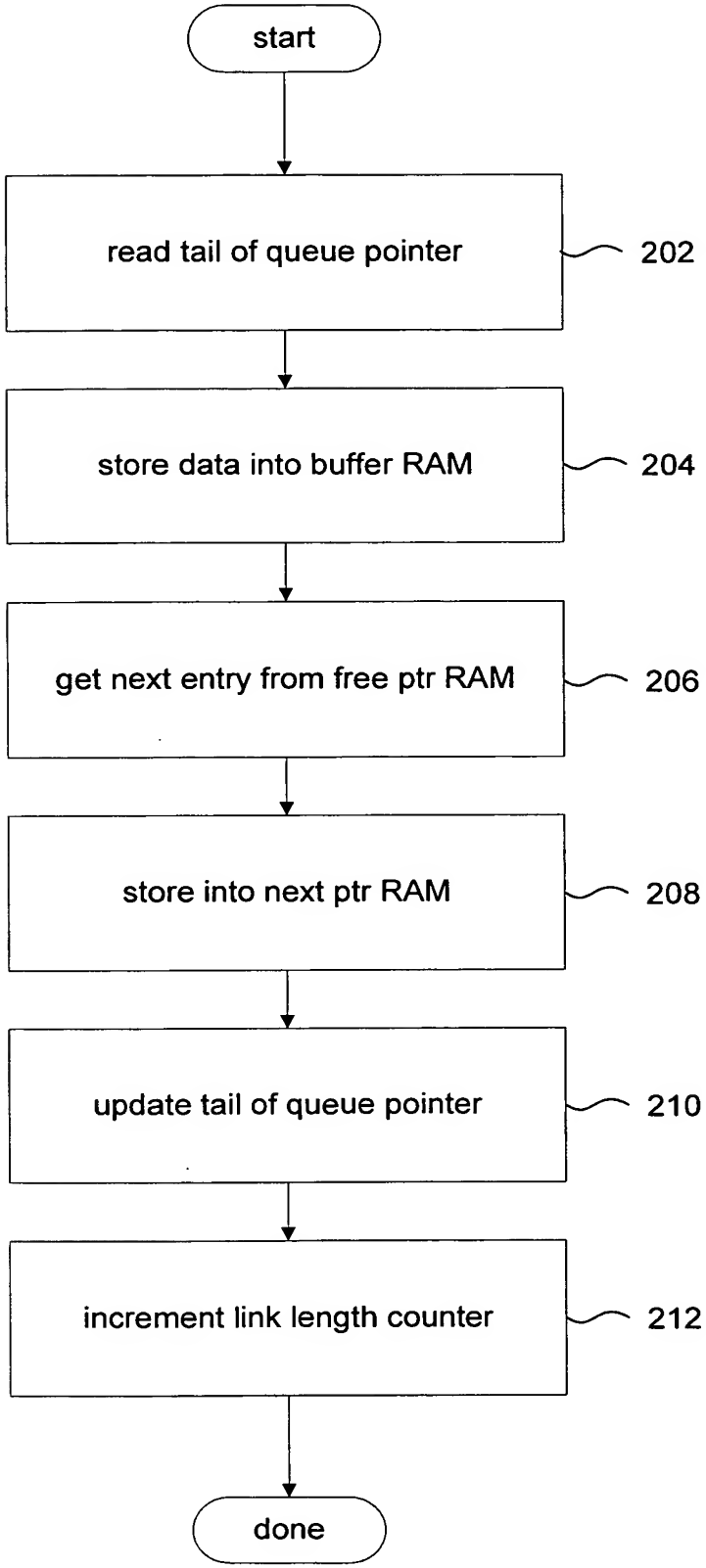
start
read tail of queue pointer
202
store data into buffer RAM
204
get next entry from free ptr RAM
206
store into next ptr RAM
208
update tail of queue pointer
210
increment link length counter
212
done

Fig. 2
(write)

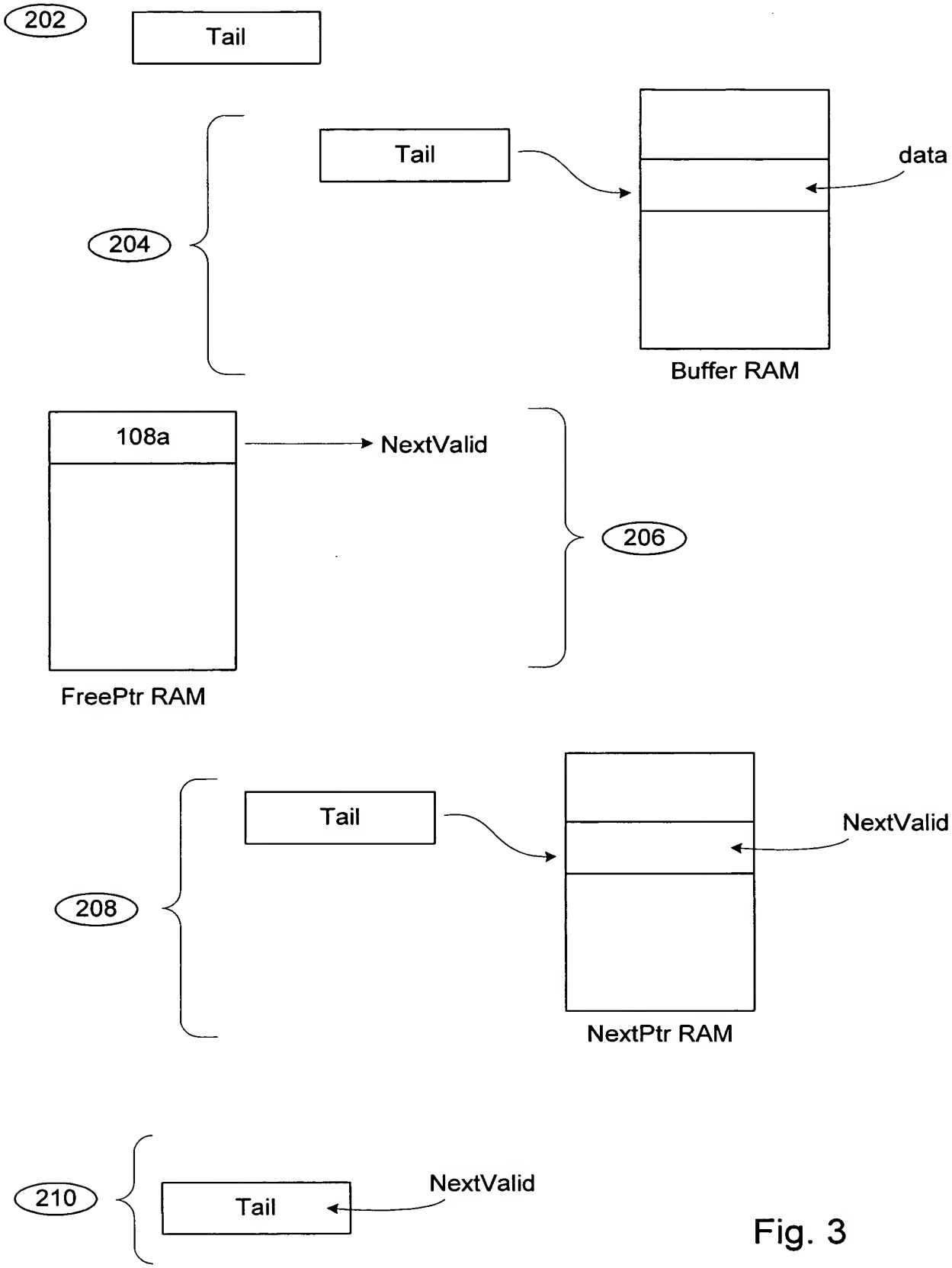
202
Tail
Tail
data
204
Buffer RAM
108a
NextValid
206
FreePtr RAM
Tail
NextValid
208
NextPtr RAM
210
Tail
NextValid

Fig. 3

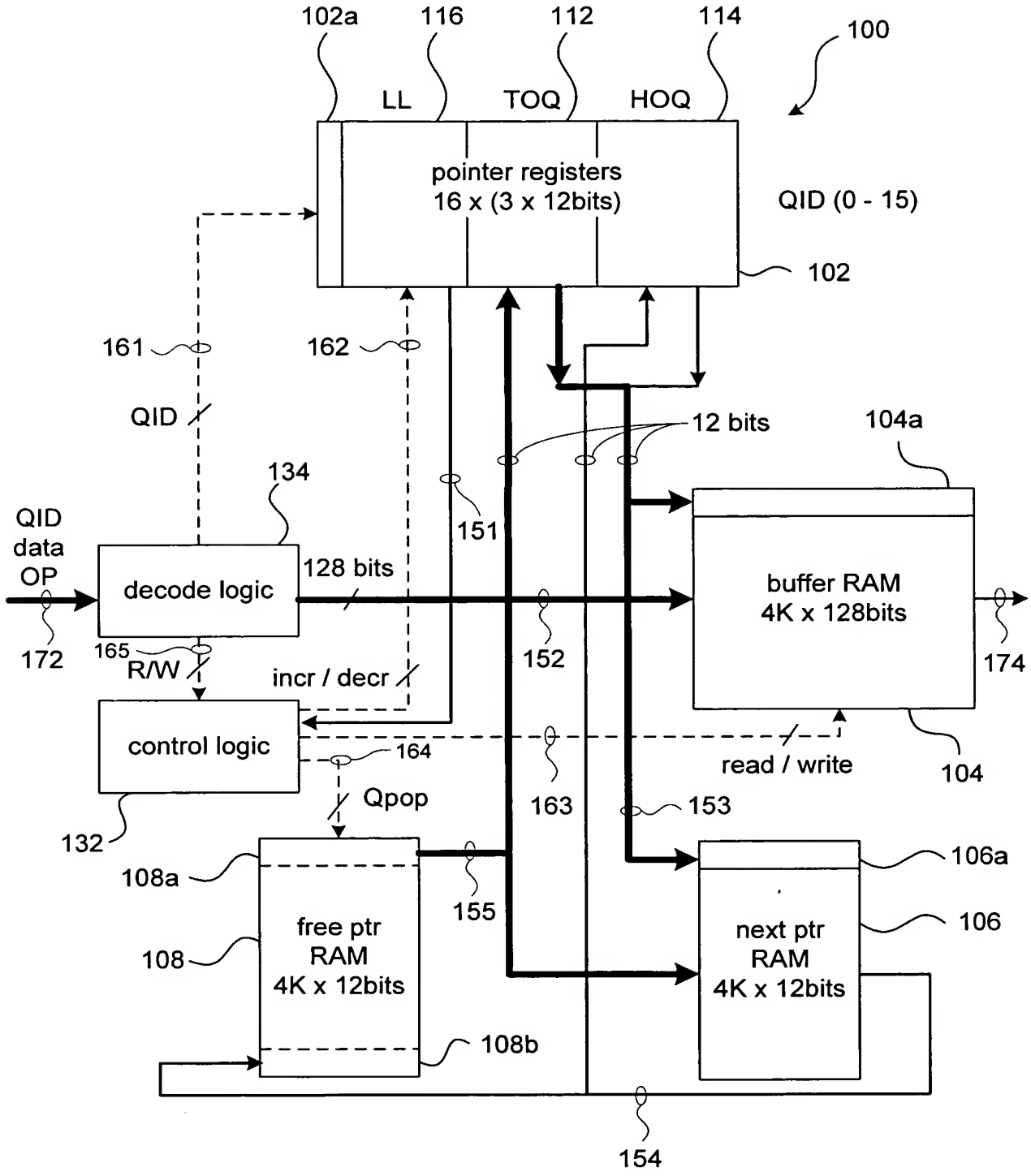
102a
116
112
114
100
LL
TOQ
HOQ
pointer registers
16 x (3 x 12bits)
QID (0 - 15)
102
161
162
QID
12 bits
104a
134
QID
data
OP
151
decode logic
128 bits
buffer RAM
4K x 128bits
172
165
R/W
incr / decr
152
174
control logic
164
read / write
104
Qpop
163
153
132
108a
106a
155
free ptr
RAM
4K x 12bits
next ptr
RAM
4K x 12bits
106
108
108b
154

Fig. 4
(write)

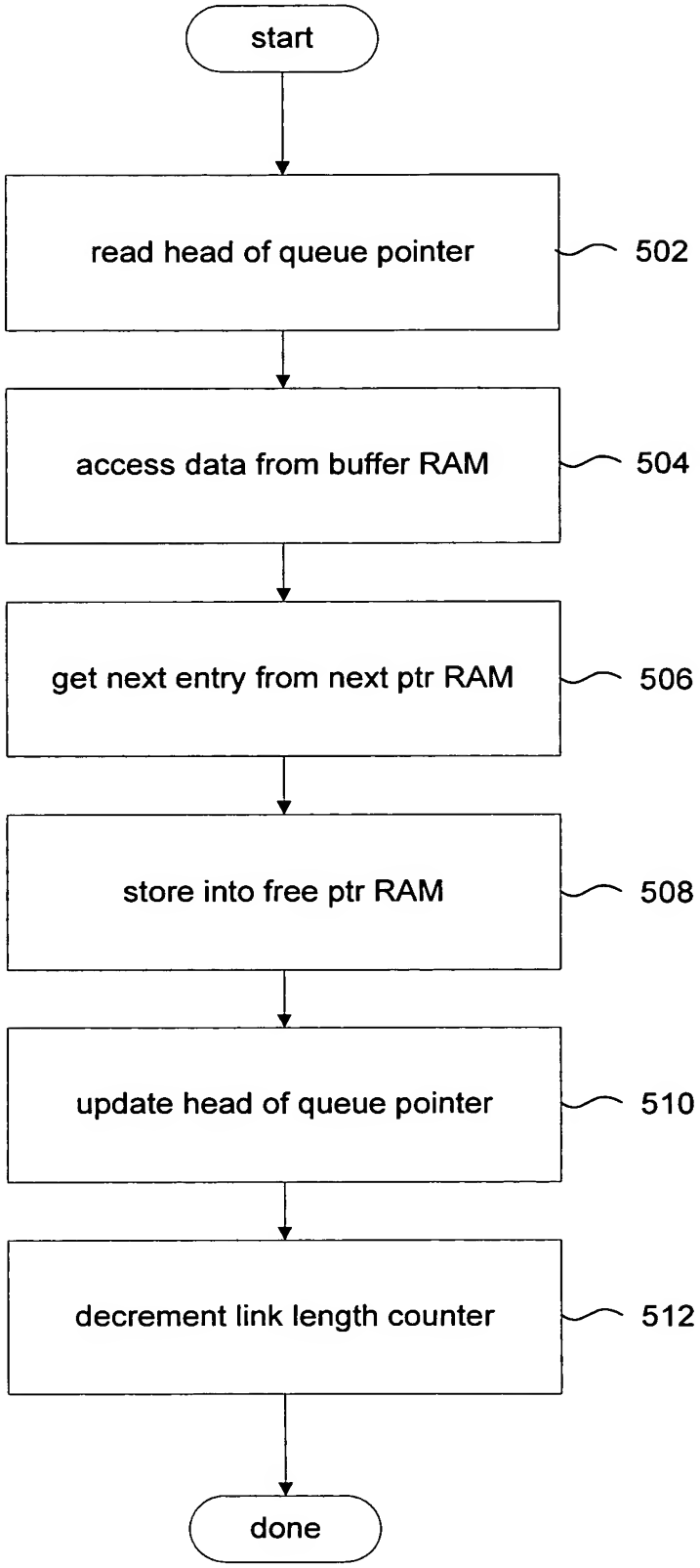
start
read head of queue pointer
502
access data from buffer RAM
504
get next entry from next ptr RAM
506
store into free ptr RAM
508
update head of queue pointer
510
decrement link length counter
512
done

Fig. 5
(read)

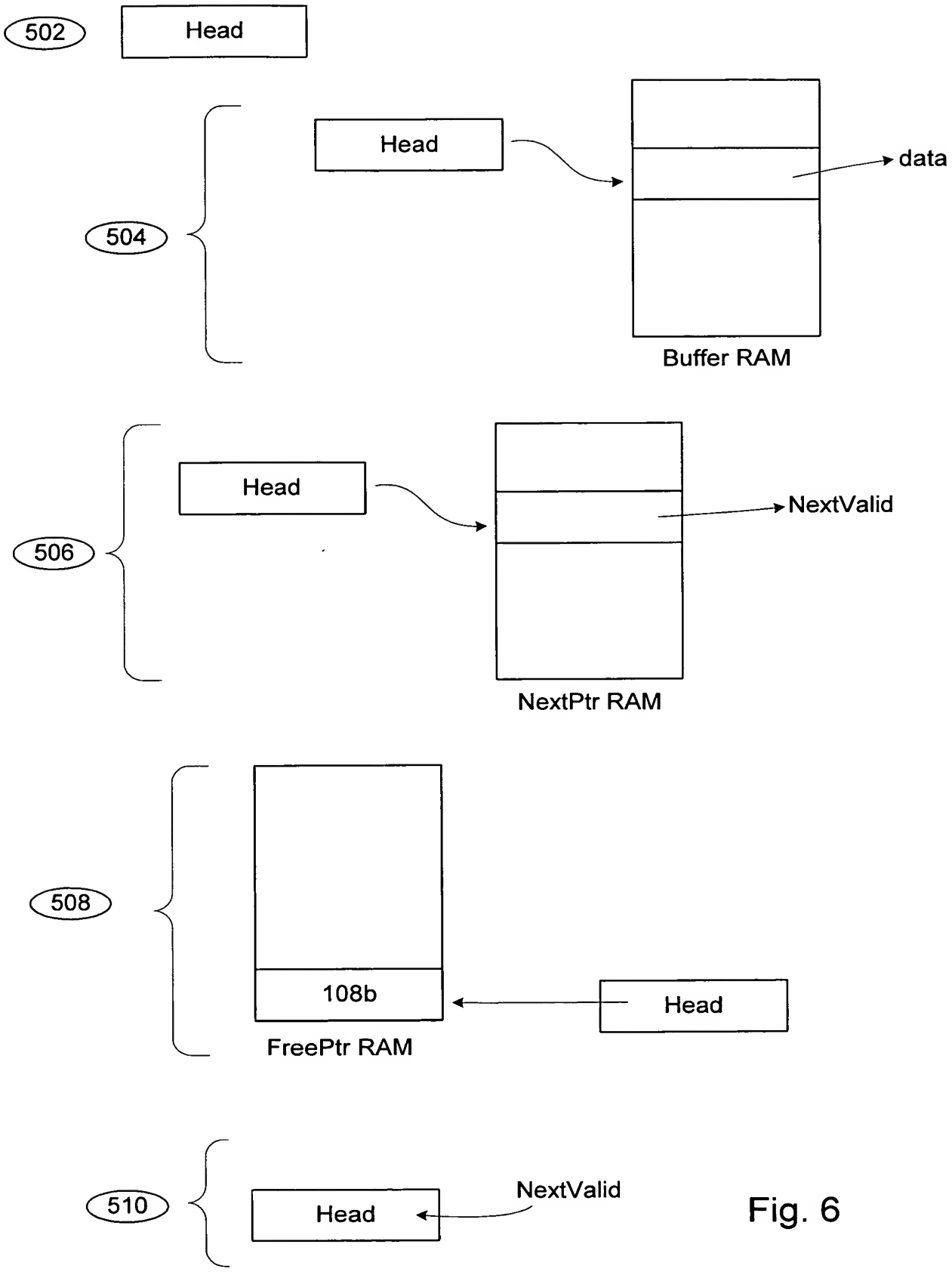
502
Head
504
Head
data
Buffer RAM
506
Head
NextValid
NextPtr RAM
508
108b
Head
FreePtr RAM
510
Head
NextValid

Fig. 6

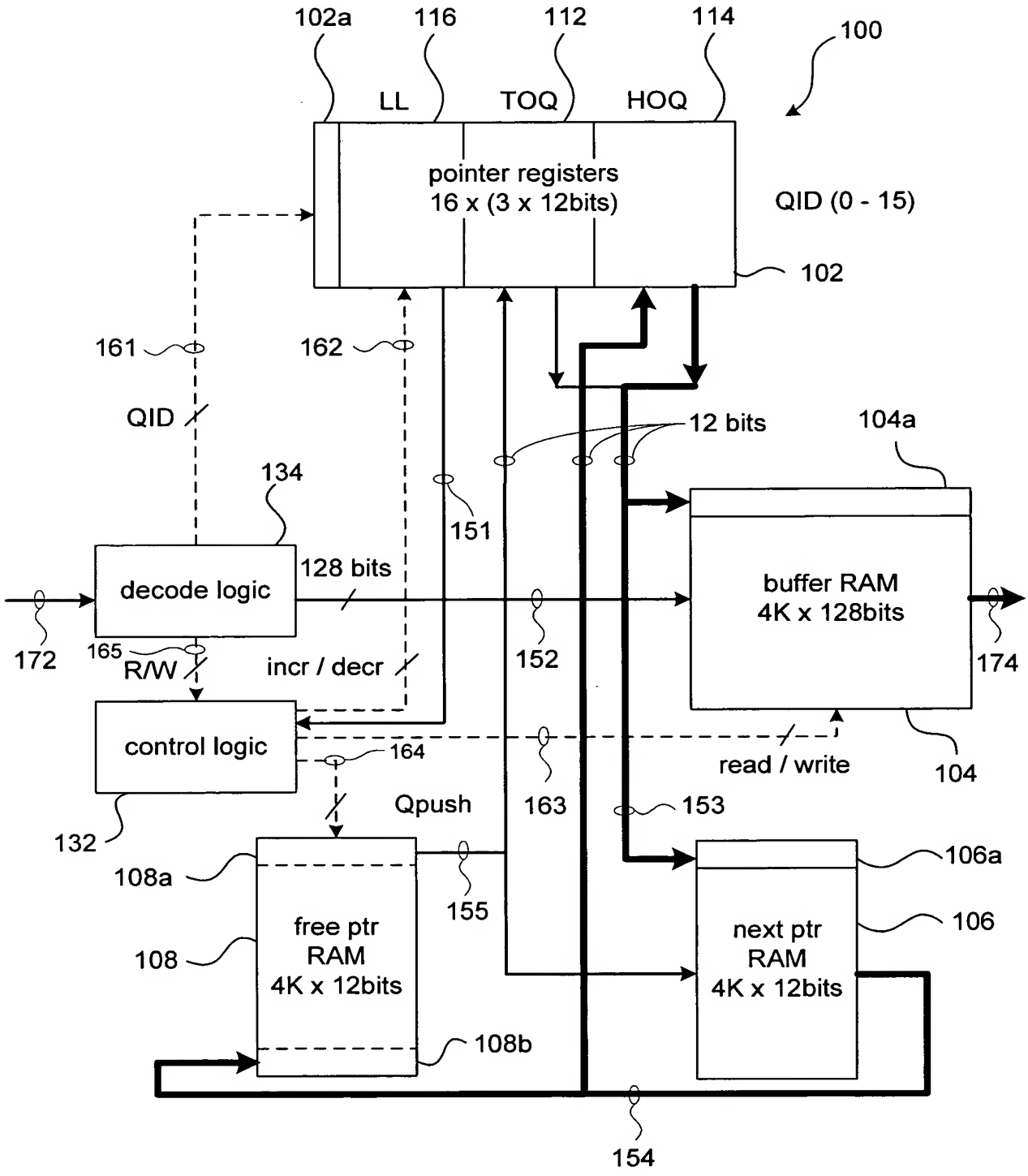
102a
116
112
114
100
LL
TOQ
HOQ
pointer registers
16 x (3 x 12bits)
QID (0 - 15)
102
161
162
QID
12 bits
104a
134
151
decode logic
128 bits
buffer RAM
4K x 128bits
172
165
R/W
incr / decr
152
174
control logic
164
read / write
104
Qpush
163
153
132
108a
106a
155
free ptr
RAM
4K x 12bits
next ptr
RAM
4K x 12bits
106
108
108b
154

Fig. 7
(read)

Initial condition

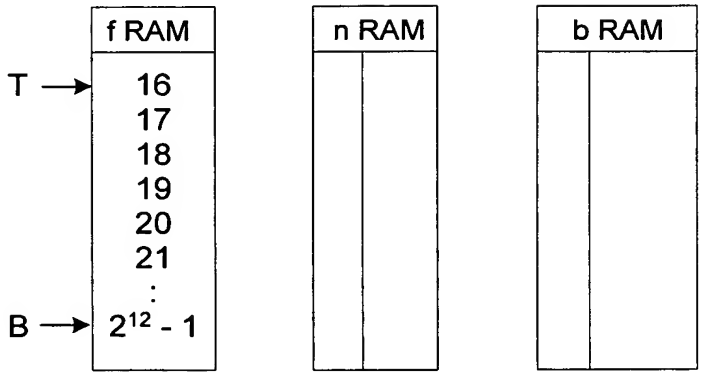

Fig. 8A

T1 = 1
bRAM (1) ← data1
pop fRAM = 16
nRAM(1) ← 16
T1 ← 16

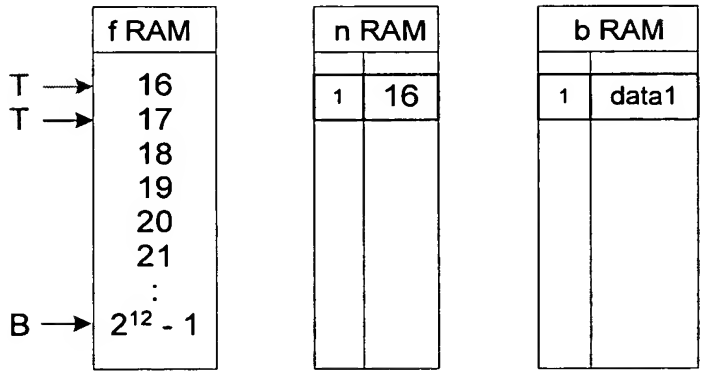

Fig. 8B

T1 = 16
bRAM (16) ← data2
pop fRAM = 17
nRAM(16) ← 17
T1 ← 17

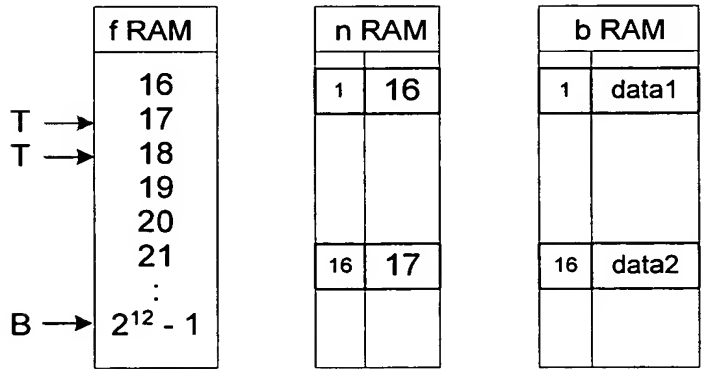

Fig. 8C

T3 = 3
bRAM (3) ← data3
pop fRAM = 18
nRAM(3) ← 18
T3 ← 18

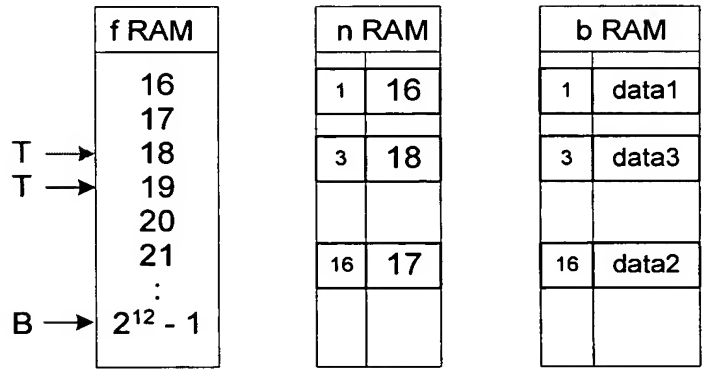

Fig. 8D

T1 = 17
bRAM (17) ← data4
pop fRAM = 19
nRAM(17) ← 19
T1 ← 19

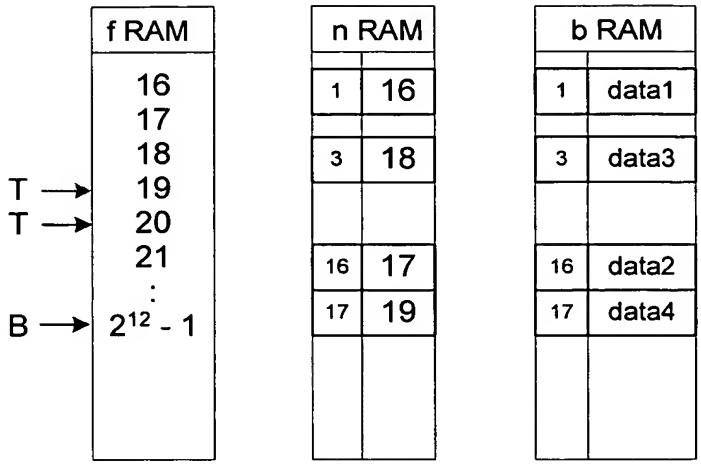

Fig. 8E

T3 = 18
bRAM (18) ← data5
pop fRAM = 20
nRAM(18) ← 20
T3 ← 20

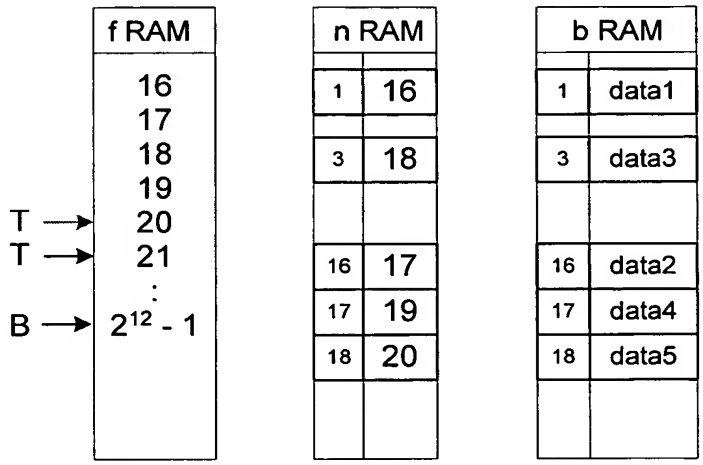

Fig. 8F

H1 = 1
bRAM (1) = data1
nRAM(1) = 16
fRAM ← H1 (push)
H1 ← 16

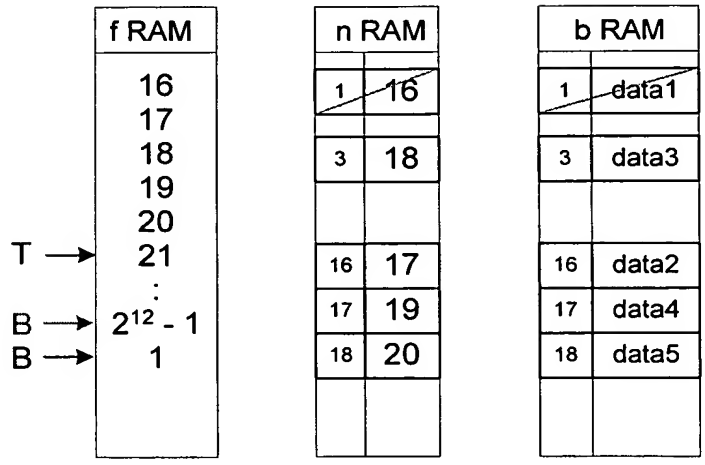

Fig. 8G

H3 = 3
bRAM (3) = data3
nRAM(3) = 18
fRAM ← H3 (push)
H3 ← 18

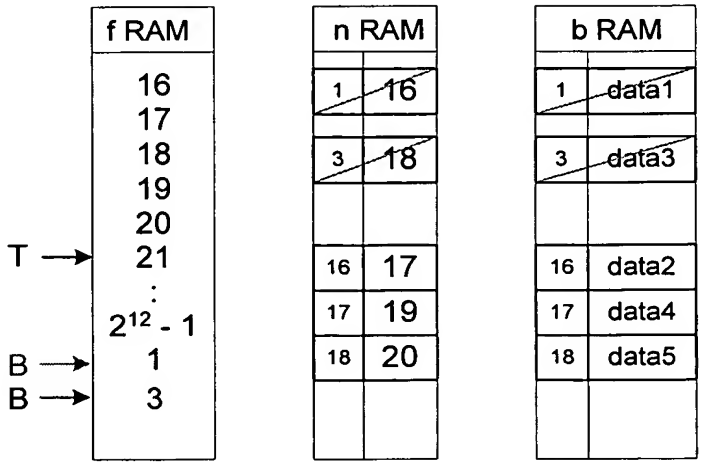

Fig. 8H

H3 = 18
bRAM (18) = data5
nRAM(18) = 20
fRAM ← H3 (push)
H3 ← 20

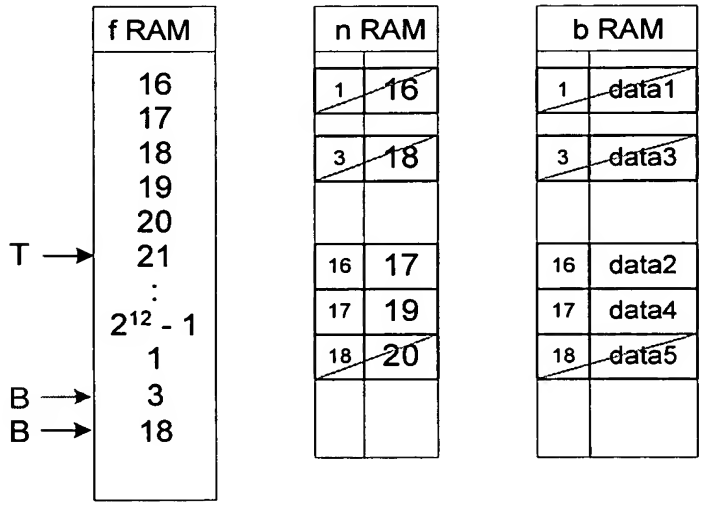

Fig. 8I

T1 = 19
bRAM (19) ← data6
pop fRAM = 21
nRAM(19) ← 21
T1 ← 21

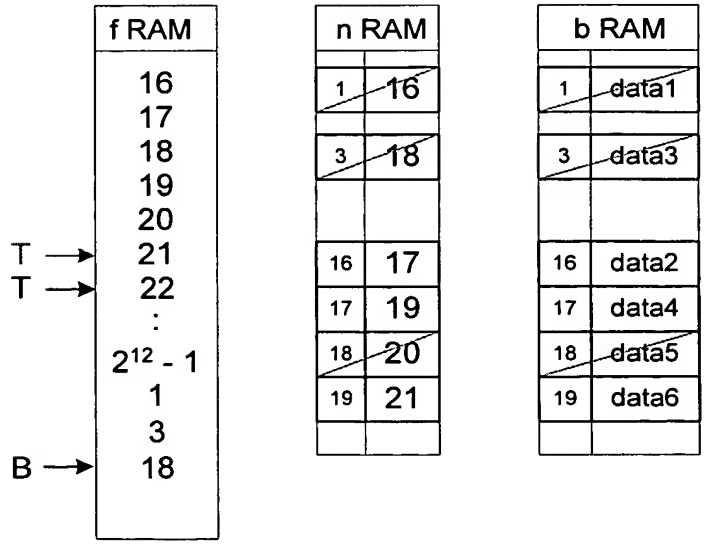

Fig. 8J